REMARKS

The specification has been amended to place it in proper idiomatic English.

In regard to the abstract, it should be noted that the abstract was placed in proper United States form in the Preliminary Amendment.

Claims 1-12 have been amended to more clearly define the invention and to remove all objections as to form.

As amended, the claims now standing in the case, are considered to be free of all objections as to form and to define the invention with the particularity required by 35 U.S.C. 112, second paragraph.

More specifically, Claims 1-12, as amended, are considered to be free of all objections made by the Examiner and to be free of all terminology which the Examiner considered to have made the claims rejectable under 35 U.S.C. 112, second paragraph as being indefinite.

The rejection of Claims 1, 2, 6, 8 11 and 12 under 35 U.S.C. 102(b) as anticipated by Findikoglu et al. is considered to lack merit.

The Findikoglu et al. patent is not considered to teach, or even suggest, the components defined by Claims 1, 2, 6 and 8 and the devices defined by Claims 11 and 12. Unlike the components

defined by Claims 1, 2, 6 and 8 and the devices defined by Claims 11 and 12, in the component and device of the Findikoglu et al. patent the electrode having a surface on the substrate is not an electrode comprising a metal or an alloy but is an electrode formed of an oxide superconductor.

The rejection of Claims 1, 9 and 10 under 35 U.S.C. 102(e) as anticipated by Mueller et al. is considered to lack merit.

The Mueller et al. patent is not considered to teach, or even suggest, the component define by Claim 1 and the devices defined by Claims 9 and 1. Unlike these component and devices, in the component of the Mueller et al. patent there is no electrode having a first surface provided on a substrate and having a dielectric provided on a second surface opposed to the second surface. Instead, in the component of the Mueller et al patent, the electrode (128b), considered by the Examiner to be a first electrode, is shown in Figs 4 and 5 and column 6, lines 46-54, to have a first surface provided on a dielectric material (124), upon a second surface of which a second electrode (128a) is provided but, is not shown to have a second surface, opposed to the first surface, provided on a substrate.

The rejection of Claim 7 under 35 U.S.C. 103 (b) as unpatentable over Findkoglu et al. is considered to lack merit.

The component defined by Claim 7 is considered to be neither shown nor suggested by the Findkoglu et al. patent for reasons

given in regard to parent Claim 1.

The rejection of Claims 3-5 under 35 U.S.C. 103(a) as unpatentable over Mueller et al is considered to lack merit.

The component defined by Claims 3-5 is considered to be neither shown nor suggested by the Mueller et al. patent for reasons given in regard to parent Claim 1. In addition, there is no teaching, or even any suggestion, in this patent of any of the electrodes shown therein being formed of at least two electrically conductive layers as in the components defined by the instant claims. It is requested that the Examiner supply evidence from the prior art to support his contention that it would have been obvious, to a person of ordinary skill in the art at the time the invention was made to form the first electrode of a first and a second layer.

An early allowance of the claims and case is requested.

Respectfully submitted,

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APPENDIX 1

The invention relates to a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed thereon, at least a dielectric disposed thereon, and at least a second electrode disposed thereon. The invention also relates to components in which at least one ceramic passive component with the above construction is used.

Variable-capacitance diodes (also called varicaps) are diodes in which the voltage dependence of a pn junction is utilized in practice. Each pn junction forms a capacitor with the p- and the n-zone as the plates and the interposed depletion or blocking layer as the dielectric. The thickness of the depletion layer increases with the applied reverse voltage, so that the capacitance value of the pn junction decreases.

Variable-capacitance diodes are available in various embodiments. Typical operating voltages are 12 to 30 V accompanied by a capacitance which is variable by a factor 10 to 20. Lower voltages in a range from 3 to 5 V are usual in mobile telephone applications with a tuning range having a factor between 2 and 4. The capacitance values of the diodes usually vary between 20 and 40 pF in this case. These semiconductor components are used inter alia in the manufacture of voltage-controlled oscillators (VCOs).

The present trend is towards lower voltages and high frequencies (GHz) especially in the field of mobile telephony. The construction of variable-capacitance diodes for this application, however, becomes increasingly difficult, especially if the dimensions of the components have to be as small as possible. The semiconductor components also come close to the limits of their possibilities in view of their effective series resistance. In addition, the cost of manufacture of variable-capacitance diodes is very high.

The invention has for its object to provide a component which has a tunable capacitance as well as a low effective series resistance and which can be inexpensively manufactured.

This object is achieved by means of a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed [thereon,] <u>on the substrate</u> at least a dielectric disposed [thereon,] <u>on the first electrode</u> and at least a second electrode disposed [thereon,] <u>on the dielectric</u> wherein the dielectric comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ε_r .

Given certain geometric dimensions (surface area A, electrode spacing d), the capacitance of a capacitor can be calculated from the equation:

$$C = (\varepsilon_r \cdot \varepsilon_0 \cdot A)/d.$$

A voltage dependence of the capacitance C is thus defined by the voltage dependence of the dielectric constant ε_r . Many dielectric materials exhibit a low dielectric constant ε_r and a low field dependence $\varepsilon_r(E)$. An exception is formed by ferroelectric materials, in which ε_r can be changed through the application of an electric field E. The capacitance value C of a capacitor can thus be changed through the application of a voltage to the electrodes.

The advantages of these components are that on the one hand they are not polar, in contrast to variable-capacitance diodes, and on the other hand that they can be manufactured more cheaply than the semiconductor components.

It is to be highly preferred that the following is chosen as the ferroelectric ceramic material with a voltage-dependent dielectric constant ε_r is chosen from the following group of materials:

$Pb(Zr_xTi_{1-x})O_3$ $(0 \leq x \leq 1)$ with and without excess lead, $Ba_{1-x}Sr_xTiO_3$ $(0 \leq x \leq 1)$,

$Pb_{1-1.5y}La_y(Zr_xTi_{1-x})O_3$ $(0 \leq x \leq 1, 0 \leq y \leq 0.2)$, $Pb(Zr_xTi_{1-x})O_3$ $(0 \leq x \leq 1)$ doped with Nb, $Pb_{1-\alpha y}La_yTiO_3$ $(0 \leq y \leq 0.3, 1.3 \leq \alpha \leq 1.5)$, $(Pb,Ca)TiO_3$, $BaTiO_3$ with and without dopants, $SrZr_xTi_{1-x}O_3$ $(0 \leq x \leq 1)$ with and without Mn dopants, $BaZr_xTi_{1-x}O_3$ $(0 \leq x \leq 1)$, $SrTiO_3$ doped with, for example, La, Nb, Fe or Mn,

$[Pb(Mg_{1/3}Nb_{2/3})O_3]_x-[PbTiO_3]_{1-x}$ $(0 \leq x \leq 1)$,

$(Pb,Ba,Sr)(Mg_{1/3}Nb_{2/3})_xTi_y(Zn_{1/3}Nb_{2/3})_{1-x-y}O_3$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $x + y \leq 1$), $PbNb_{4/5x}((Zr_{0.6}Sn_{0.4})_{1-y}Ti_y))_{1-x}O_3$ ($0 \leq x \leq 0.9$, $0 \leq y \leq 1$), $(Ba_{1-x}Ca_x)TiO_3$ ($0 \leq x \leq 1$),

$(Ba_{1-x}Sr_x)TiO_3$ ($0 \leq x \leq 1$), $(Ba_{1-x}Pb_x)TiO_3$ ($0 \leq x \leq 1$), $(Ba_{1-x}Sr_x)(Ti_{1-x}Zr_x)O_3$

($0 \leq x \leq 1$, $0 \leq y \leq 1$),

a) $Pb(Mg_{1/2}W_{1/2})O_3$

b) $Pb(Fe_{1/2}Nb_{1/2})O_3$

c) $Pb(Fe_{2/3}W_{1/3})O_3$

d) $Pb(Ni_{1/3}Nb_{2/3})O_3$

e) $Pb(Zn_{1/3}Nb_{2/3})O_3$

f) $Pb(Sc_{1/2}Ta_{1/2})O_3$

as well as combinations of the compounds a) to f) with $PbTiO_3$ and $Pb(Mg_{1/3}Nb_{2/3})O_3$ with and without excess lead.

All these ferroelectric ceramic materials have a high, voltage-dependent relative dielectric constant ε_r.

In another preferred embodiment, the first electrode and/or the second electrode comprise(s) at least a first and a second electrically conducting layer.

It is preferred that the first electrically conducting layer of the electrodes comprises Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$). These layers serve as adhesion layers.

It is furthermore preferred that the second electrically conducting layer of the electrodes comprises a metal or an alloy.

The electric current is mainly passed by the second, well conducting layer. A high conductivity of the materials used leads to a low effective series resistance (ESR) and a low parasitic inductance (ESL).

In a preferred embodiment [it is provided that] the carrier substrate comprises a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, a glass material, or silicon.

A carrier substrate made of a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, or a glass material can be inexpensively manufactured, so that the process cost for these components can be kept low. If the passive ceramic component is integrated into an IC, the carrier substrate will be formed of silicon, possibly provided with an SiO_2 passivating layer.

A further preferred embodiment is characterized in that the dielectric comprises multiple layers.

The use of multiple layers, for example double, triple or quadruple layers renders it possible to compensate for the unfavorable temperature behavior of some ferroelectric materials and to improve the temperature dependence of the capacitance value C.

It is also preferred that a protective layer of an inorganic material and/or an organic material is laid over the entire component.

The protective layer protects the subjacent layers against mechanical loads and against corrosion caused by moisture.

The invention also relates to components, in particular tunable filters [or] delay lines or voltage-controlled oscillators, which comprise as their capacitive component a ceramic passive component which comprises a carrier substrate, at least a first electrode disposed [thereon,] on the substrate at least a dielectric disposed [thereon,] on the first electrode, and at least a second electrode disposed [thereon,] on the dielectric, [which is characterized in that] in which the dielectric comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ε_r.

The use of the component according to the invention, for example, in a tunable RCL filter, a passive delay line with electrically tunable delay time, or as a replacement for a variable-capacitance diode in voltage-controlled oscillators is advantageous because the component according to the invention can be mounted together with other components on a substrate, so that inexpensive circuits of small constructional dimensions can be manufactured.

The invention furthermore relates to the use as a capacitive component of a ceramic passive component which comprises

a carrier substrate, at least a first electrode disposed [thereon,] on the substrate at least a dielectric with a voltage-dependent relative dielectric constant ε_r disposed [thereon,] on the first electrode and at least a second electrode disposed [thereon,] on the dielectric [as a capacitive component].

The invention will be explained in more detail below with reference to five Figures and three embodiments, where

Fig. 1 in a diagrammatic, cross-sectional view shows the construction of a ceramic passive component of the invention,

Fig. 2 [plots] is a graph of the capacitance as a function of the applied voltage in a ceramic passive component according to the invention,

Fig. 3 is the circuit diagram of an RCL filter,

Fig. 4 shows the filter characteristic of an RCL filter which comprises a component according to the invention as its capacitive component, and

Fig. 5 is the circuit diagram of a passive LC delay member.

In Fig. 1, a ceramic passive component comprises a carrier substrate1 which is made, for example, from a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, a glass material, or silicon with a passivating layer. On the carrier substrate there is a first electrode 2 which comprises a first electrically conducting layer 3

of, for example, Ti, Cr, Ni_xCr_y ($0 \le x \le 1$, $0 \le y \le 1$) or Ti_xW_y ($0 \le x \le 1$, $0 \le y \le 1$) and a second elecrically conducting layer 4 comprising, for example, Pt, Ag, Ir, $Ag_{1-x}Pt_x$ ($0 \le x \le 1$), Ni, Cu, W, $Ag_{1-x}Pd_x$ ($0 \le x \le 1$), Al, Al doped with Cu, Al doped with Si or Al doped with Mg. A dielectric 5, for example made of a material made of $Pb(Zr_xTi_{1-x})O_3$ ($0 \le x \le 1$) with and without excess lead, $Ba_{1-x}Sr_xTiO_3$ ($0 \le x \le 1$),

$Pb_{1-1.5y}La_y(Zr_xTi_{1-x})O_3$ ($0 \le x \le 1$, $0 \le y \le 0.2$), $Pb(Zr_xTi_{1-x})O_3$ ($0 \le x \le 1$) doped with Nb, $Pb_{1-\alpha y}La_yTiO_3$ ($0 \le y \le 0.3$, $1.3 \le \alpha \le 1.5$), $(Pb,Ca)TiO_3$, $BaTiO_3$ with and without dopants, $SrZr_xTi_{1-x}O_3$ ($0 \le x \le 1$)with and without Mn dopants, $BaZr_xTi_{1-x}O_3$ ($0 \le x \le 1$), $SrTiO_3$ doped with, for example, La, Nb, Fe or Mn,

$[Pb(Mg_{1/3}Nb_{2/3})O_3]_x-[PbTiO_3]_{1-x}$ ($0 \le x \le 1$),

$(Pb,Ba,Sr)(Mg_{1/3}Nb_{2/3})_xTi_y(Zn_{1/3}Nb_{2/3})_{1-x-y}O_3$ ($0 \le x \le 1$, $0 \le y \le 1$, $x + y \le 1$), $PbNb_{4/5x}((Zr_{0.6}Sn_{0.4})_{1-y}Ti_y))_{1-x}O_3$ ($0 \le x \le 0.9$, $0 \le y \le 1$), $(Ba_{1-x}Ca_x)TiO_3$ ($0 \le x \le 1$),

$(Ba_{1-x}Sr_x)TiO_3$ ($0 \le x \le 1$), $(Ba_{1-x}Pb_x)TiO_3$ ($0 \le x \le 1$), $(Ba_{1-x}Sr_x)(Ti_{1-x}Zr_x)O_3$

($0 \le x \le 1$, $0 \le y \le 1$),

a) $Pb(Mg_{1/2}W_{1/2})O_3$

b) $Pb(Fe_{1/2}Nb_{1/2})O_3$

c) $Pb(Fe_{2/3}W_{1/3})O_3$

d) $Pb(Ni_{1/3}Nb_{2/3})O_3$

e) $Pb(Zn_{1/3}Nb_{2/3})O_3$

f) $Pb(Sc_{1/2}Ta_{1/2})O_3$

as well as combinations of the compounds a) to f) with $PbTiO_3$ and $Pb(Mg_{1/3}Nb_{2/3})O_3$ with and without excess lead is provided on the first electrode 2. On the dielectric 5 there is a second electrode 6 which is made of, for example, Pt, Ag, Ir, $Ag_{1-x}Pt_x$ ($0 \leq x \leq 1$), Ni, Cu, W, $Ag_{1-x}Pd_x$ ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si or Al doped with Mg or YBa_2CuO_x. A protective layer 7 of an organic and/or inorganic material is provided over the second electrode 6. The organic material used may be, for example, polybenzocyclobutene or polyimide, and the inorganic material may be, for example, Si_3N_4, SiO_2 or $Si_xO_yN_z$ ($0 \leq x \leq 1$, $0 \leq y \leq 1$, $0 \leq z \leq 1$).

Alternatively, the first electrode 2 may comprise only one electrically conducting layer of, for example, Pt, Ag, Ir, $Ag_{1-x}Pt_x$ ($0 \leq x \leq 1$), Ni, Cu, W, $Ag_{1-x}Pd_x$ ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si, or Al doped with Mg, or YBa_2CuO_x . In addition, the second electrode 6 may comprise at least a first and a second electrically conducting layer. The first electrically conducting layer may then comprise, for example, Ti, Cr, Ni_xCr_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$) or Ti_xW_y ($0 \leq x \leq 1$, $0 \leq y \leq 1$). The material used for the second electrically conducting layer may be, for example, Pt, Ag, Ir, $Ag_{1-x}Pt_x$ ($0 \leq x \leq 1$), Ni, Cu, W, $Ag_{1-x}Pd_x$ ($0 \leq x \leq 1$), Al, Al doped with Cu, Al doped with Si or Al doped with Mg .

[Yet further, for example] Additionally, third, fourth, and fifth electrically conducting layers may be provided on the respective second electrically conducting layers of the electrodes 2 and 6 as long as suitable combinations of the individual materials are formed. Materials which are suitable for forming a third electrically conducting layer are, for example, Ti, Ir, Ag, Cr, Al, IrO_x ($0 \le x \le 2$), Ru, Ru_xPt_{1-x} ($0 \le x \le 1$), Pt_xAl_{1-x} ($0 \le x \le 1$), RhO_x ($0 \le x \le 2$), Pt_xRh_{1-x} ($0 \le x \le 1$), or ITO. A fourth electrically conducting layer may comprise, for example, IrO_x ($0 \le x \le 2$), RuO_x ($0 \le x \le 2$), Ru_xPt_{1-x} ($0 \le x \le 1$), Pt_xAl_{1-x} ($0 \le x \le 1$), RhO_x ($0 \le x \le 2$), Pt_xRh_{1-x} ($0 \le x \le 1$), or ITO. A fifth electrically conducting layer may be formed from, for example, RuO_x ($0 \le x \le 2$) or Ru_xPt_{1-x} ($0 \le x \le 1$).

At least a first and a second current supply contact may be provided at [eitheer] either side of the ceramic passive component. A current supply contact may be, for example, an electroplated SMD end contact of Cr/Cu, Ni/Sn or Cr/Cu, Cu/Ni/Sn or Cr/Ni, Pb/Sn or a bump end contact or a contact surface.

The dielectric 5 may also comprise multiple layers, for example double, triple, or quadruple layers.

Furthermore, an anti-reaction layer made of, for example, TiO_2, Al_2O_3, $ZrTiO_4$ or ZrO_2 may be deposited on the carrier substrate 1. If silicon [was] used for the carrier substrate 1, the carrier substrate 1 may be provided with an SiO_2 passivating layer.

Fig. 3 shows an RCL filter arrangement consisting of a capacitor C1 with a defined capacitance value, a tunable capacitor C2, two resistors R1 and R2, and three inductances L1 to L3. The RCL filter comprises a first series arrangement of a resistor R1, an inductance L1, and a capacitor C1 connected in parallel to a second series arrangement of a resistor R2, an inductance L2, and a capacitor C2. The inductance L3 is connected in series with this parallel circuit and has one of its terminals connected to ground potential. The parallel circuit is thus [connectd] connected at one side to the inductance L3, while both the potential V_t and the connection terminals 8 and 9 are applied to the other side.

Fig. 5 shows the circuit arrangement of a passive LC delay member consisting of an inductance L4 and a capacitor C4 which are connected to one another. The junction point between the inductance L4 and the capacitor C4 is connected to a tap 10 and has potential V_t. The other connection is at a tap 11. The other terminal of the capacitor C4 is at ground potential.

Embodiments of the invention will be explained in more detail below, showing examples of how the invention may be carried into practice.

First an anti-reaction layer of TiO_2 and then a first electrically conducting layer 3 of Ti (10 nm) were deposited on a carrier substrate 1 of Al_2O_3 with a glass palanarization layer. A

second electrically conducting layer 4 of Pt (500 nm) was deposited by sputtering on this first electrically conducting layer 3, and the two layers were structured by photolithography. Subsequently, a dielectric 5 of $PbZz_{0.53}Ti_{0.47}O_3$ with 5% La [dotation] dopation was deposited in a sol-gel process, tempered at approximately 600 °C in an oxygen atmosphere, and structured by photolithography. The thickness of the dielectric was 0.75 µm. In the next step, a 500 nm Pt layer was deposited and structured photolithographically into an electrode 6. A protective layer 7 of Si_3N_4 and a polyimide was deposited over the entire component. In addition, Cr/Cu, Ni/Sn SMD end contacts were fastened on mutually opposed sides of the component so as to serve as current supply contacts.

Fig. 2 shows the gradient of the capacitance of the ceramic passive component as a function of the applied voltage.

To achieve the same tuning range for the capacitance at lower voltages than those shown in Fig.2, ceramic passive components with a thickness of the dielectric 5 of d = 0.25 µm were manufactured in the manner indicated above. At a surface capacitance of 28 nF/mm^2 , a ceramic passive component with a capacitance of 50 pF on an active surface area of approximately 1800 µm^2 (42.5 µm * 42.5 µm) was manufactured, as well as a ceramic passive component with a capacitance of 5 pF on an active surface area of approximately 180 µm^2 (13.4 µm * 13.4 µm).

The ceramic passive components thus formed were used in mobile telephones instead of variable-[capcitance] capacitance diodes.

A ceramic passive component was manufactured by the method as explained with reference to Embodiment 1 with a capacitance which was tunable in a range from 17 pF to 56 pF.

This ceramic passive component was used for realizing a tunable RCL filter which is to show a strong damping either at 900 MHz or at 1800 MHz. A capacitor C1 with a defined capacitance value and a tunable capacitor C2 were for this purpose combined with two resistors R1 and R2 and three inductances L1 to L3 into an RCL combination in accordance with the circuit arrangement of Fig. 3. The following were the values:

R1 = 5 Ω, L1 = 0.26 nH, C1 = 2.8 nF, and

R2 = 0.5 Ω, L2 = 0.26 nH, C2 = variable between 17 and 56 pF, and

L3 = 0.3 nH.

The application of a DC voltage of a few volts is capable of varying the capacitance value of the capacitor C2 between 17 and 56 pF, whereby the region having a strong absorption in the filter characteristic can be shifted back and forth between 900 and 1800 MHz, as is shown in Fig. 4. Curve I in this Fig. corresponds to a capacitance value of the capacitor C2 of 56 pF and curve II to a capacitance value of 17 pF.

A ceramic passive component was manufactured by the method as explained with reference to Embodiment 1 with a capacitance which was tunable in a range from 1.4 nF to 2.8 nF through the application of a DC voltage of a few volts.

[The] This ceramic passive component was used in [for realizing] a passive LC delay member with an electrically changeable delay time t_d . The tunable capacitor C4 was for this purpose combined with an inductance L4 of 5.7 nH, as shown in Fig. 5.

The delay time t_d , which is given by: $t_d = \sqrt{L*C}$, can be shortened from 4 ns at a capacitance value of 2.8 nF to 2.8 ns in that the capacitance is changed to 1.4 nF.

APPENDIX 11

1. (Amended) A ceramic passive component which comprises a carrier substrate (1),

at least one [a] first electrode comprising a metal or alloy and (2) having a first surface disposed [thereon],

on the substrate at least one [a] dielectric (5) having a first surface disposed [thereon], on a second surface of the at least one first electrode opposing said first surface of the at least one first electrode, and

at least a second electrode (6) disposed thereon,

characterized in that the dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ε_r .

2. (Amended) A ceramic passive component as claimed in claim 1, [characterized in that] wherein the [following is chosen as] the ferroelectric ceramic material with a voltage-dependent dielectric constant ε_r is a material selected from the group consisting of: $Pb(Zr_xTi_{1-x})O_3$ ($0 \leq x \leq 1$) with and without excess lead, $Ba_{1-x}Sr_xTiO_3$ ($0 \leq x \leq 1$),

$Pb_{1-1.5y}La_y(Zr_xTi_{1-x})O_3$ ($0 \le x \le 1$, $0 \le y \le 0.2$), $Pb(Zr_xTi_{1-x})O_3$ ($0 \le x \le 1$) doped with Nb, $Pb_{1-\alpha y}$ La_yTiO_3 ($0 \le y \le 0.3$, $1.3 \le \alpha \le 1.5$), $(Pb,Ca)TiO_3$, $BaTiO_3$ with and without dopants, $SrZr_xTi_{1-x}O_3$ ($0 \le x \le 1$) with and without Mn dopants, $BaZr_xTi_{1-x}O_3$ ($0 \le x \le 1$), $SrTiO_3$ doped with, for example, La, Nb, Fe or Mn,

$[Pb(Mg_{1/3}Nb_{2/3})O_3]_x-[PbTiO_3]_{1-x}$ ($0 \le x \le 1$),

$(Pb,Ba,Sr)(Mg_{1/3}Nb_{2/3})_xTi_y(Zn_{1/3}Nb_{2/3})_{1-x-y}O_3$ ($0 \le x \le 1$, $0 \le y \le 1$, $x + y \le 1$), $PbNb_{4/5x}((Zr_{0.6}Sn_{0.4})_{1-y}Ti_y))_{1-x}O_3$ ($0 \le x \le 0.9$, $0 \le y \le 1$), $(Ba_{1-x}Ca_x)TiO_3$ ($0 \le x \le 1$),

$(Ba_{1-x}Sr_x)TiO_3$ ($0 \le x \le 1$), $(Ba_{1-x}Pb_x)TiO_3$ ($0 \le x \le 1$), $(Ba_{1-x}Sr_x)(Ti_{1-x}Zr_x)O_3$

($0 \le x \le 1$, $0 \le y \le 1$),

[a)] $Pb(Mg_{1/2}W_{1/2})O_3$

[b)] $Pb(Fe_{1/2}Nb_{1/2})O_3$

[c)] $Pb(Fe_{2/3}W_{1/3})O_3$

[d)] $Pb(Ni_{1/3}Nb_{2/3})O_3$

[e)] $Pb(Zn_{1/3}Nb_{2/3})O_3$

[f)] $Pb(Sc_{1/2}Ta_{1/2})O_3$

as well as combinations of <u>these last six</u> [the] compounds a) to f) with $PbTiO_3$ and $Pb(Mg_{1/3}Nb_{2/3})O_3$ with and without excess lead.

3. (Amended) A ceramic passive component as claimed in claim 1, [characterized in that] <u>wherein</u> the <u>at least one</u> first electrode

(2) [and/] or the at least one second electrode (6) comprise(s) at least a first and a second electrically conducting layer.

4. (Amended) A ceramic passive component as claimed in claim 3, [characterized in that] wherein the first electrically conducting layer of the at least one first electrode (2) or of the at least one second electrode (6)[electrodes (2, 6)] comprises Ti, Cr, Ni_xCr_y $(0 \le x \le 1,\ 0 \le y \le 1)$ or Ti_xW_y $(0 \le x \le 1,\ 0 \le y \le 1)$.

5. (Amended) A ceramic passive component as claimed in claim 3, [characterized in that] wherein the second electrically conducting layer of the at least one first electrode (2) or of the at least one second electrode (6) [electrodes (2, 6)] comprises a metal or an alloy.

6. (Amended) A ceramic passive component as claimed in claim 1, [characterized in that] wherein the carrier substrate (1) comprises a ceramic material, a ceramic material with a glass planarization layer, a glass-ceramic material, a glass material, or silicon.

7. (Amended) A ceramic passive component as claimed in claim 1, [characterized in that] wherein the at least one dielectric (5) comprises multiple layers.

8. (Amended) A ceramic passive component as claimed in claim 1, [characterized in that] wherein a protective layer (7) of an inorganic material and/or an organic material is laid over the entire component.

9. (Amended) A voltage-controlled oscillator with as its capacitive component a ceramic passive component which comprises a carrier substrate (1), at least one [a] first electrode (2) comprising a metal or alloy and having a first surface disposed [thereon], on the substrate at least [a] one dielectric (5) having a first surface disposed [thereon], on a second surface, opposed to said first surface of the at least first electrode and at least a second electrode (6) disposed [thereon] on a second surface of the at least one dielectric, opposed to said first surface of the at least one dielectric, [characterized in that] wherein the at least one dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ε_r .

10. (Amended) A filter with as its capacitive component a ceramic passive component which comprises a carrier substrate (1), at least one [a] first electrode (2) comprising a metal or alloy and having a first surface disposed [thereon] on the substrate, at least [a] one dielectric (5) having a first surface disposed [thereon], the at least one first electrode opposed to said first surface, and at least [a] one second electrode (6) disposed [thereon],

on said second surface of the at least one dielectric [characterized in that] <u>wherein</u> the <u>at least one</u> dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ε_r .

11. (<u>Amended</u>) A delay line with as its capacitive component a ceramic passive component which comprises a carrier substrate (1), at least [a] <u>one</u> first electrode (2) <u>comprising a metal or alloy and having a first surface</u> disposed [thereon], <u>on the substrate</u> at least [a] <u>one</u> dielectric (5) <u>having a first surface</u> disposed [thereon], <u>on a second surface of the at least one first electrode opposed to said first surface</u>, and at least [a] one second electrode (6) <u>having a surface</u> disposed [thereon], <u>on said second surface of the at least one dielectric</u>, [characterized in that] the <u>at least one</u> dielectric (5) comprises a ferroelectric ceramic material with a voltage-dependent relative dielectric constant ε_r .

12. (<u>Amended</u>) The use of a ceramic passive component which comprises a carrier substrate (1), at least [a] <u>one</u> first electrode (2) <u>comprising a metal or alloy and having a first surface</u> disposed [thereon], <u>on the substrate</u> at least [a] <u>one</u> dielectric (5) with a voltage-dependent relative dielectric constant ε_r <u>having a second surface opposed to said first surface</u> disposed [thereon], <u>on a second surface of the at least one first electrode opposed to said</u>

first surface and at least [a] one second electrode (6) disposed [thereon] on said second surface of the at least one dielectric as a capacitive component.